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PATENT APPLICATION
Attorney's Do. No. 8750-17.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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ADRIENNE CHOCHOLAK
(SENDER'S PRINTED NAME)

(SIGNATURE)

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Enclosed for filing is a patent application under 37 CFR 1.53(b) of:

Inventor Sang-Eun LEE and Jae-Sung HAN:
For: METHOD OF IDENTIFYING AND ANALYZING SEMICONDUCTOR
CHIP DEFECTS

Applicant requests FIG. 1 to be published with the application.

Enclosures:

- | | |
|-------------------------------------|---|
| <input checked="" type="checkbox"/> | Specification (pages 1-7); claims (pages 8-10); abstract (page 11) |
| <input checked="" type="checkbox"/> | SEVEN sheet(s) of FORMAL drawings |
| <input checked="" type="checkbox"/> | Declaration or Combined Declaration and Power of Attorney |
| <input checked="" type="checkbox"/> | Newly executed (original or copy) |
| <input checked="" type="checkbox"/> | Assignment with cover sheet |
| | Assignee Name and Address: Samsung Electronics Co., Ltd.
Suwon-city, Kyungki-do, Korea |
| <input checked="" type="checkbox"/> | Certified copy of Priority Document No. 2001-8465, filed February 20, 2001 |
| <input checked="" type="checkbox"/> | Return Postcard |

<u>CLAIMS AS FILED</u>				
For	Number Filed	Number Extra	Rate	Basic Fee \$740
Total Claims	20-20	0	x \$ 18 =	0
Independent Claims	3-3	0	x \$ 84 =	0
TOTAL FILING FEE				\$740



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Any deficiency or overpayment should be charged or credited to deposit account
number 13-1703. A duplicate copy of this sheet is enclosed.



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PATENT TRADEMARK OFFICE

Respectfully submitted,

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